IN THE CLAIMS:

Please amend the claims as follows:

1. (Previously Presented) A TFT array substrate, comprising:

a display area including a pixel electrode,

a switching element connected to the pixel electrode,

a gate line connected to the switching element and a source line connected to the switching element, and

a terminal formed outside of said display area for connecting the gate line or the source line to wiring from an external signal source, wherein the terminal comprises a terminal electrode connected to said wiring from said external signal source, and a first metallic line and a second metallic line arranged beneath the terminal electrode, and each are connected to the terminal electrode via a contact hole,

wherein the first metallic line is formed in a side of the display area, and the second metallic line is formed in a side of the substrate end;

wherein the TFT array substrate further comprises an insulating layer which is interposed between the first metallic line and the second metallic line;

wherein the first metallic line is formed over the insulating layer;

wherein said second metallic line is formed beneath the insulating layer;

wherein any one of said first metallic line and said second metallic line is formed in the same layer of said source line, and the other one of said first and second metallic lines is formed in the same layer of said gate line;

wherein said first and second metallic lines are connected via a contact hole formed in a passivation film which is provided beneath the terminal electrode; and

wherein said second metallic line, which is extending from the terminal electrode to the substrate end, is formed beneath both said insulating layer and said passivation film.

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12. (Previously Presented) The TFT array substrate of claim 1, wherein the first metallic line and the terminal electrode are connected via a plurality of contact holes.

13. (Previously Presented) The TFT array substrate according to claim 1, wherein the side of the substrate end is a side where the TFT array substrate is cut off and chamfered off.

14. (Previously Presented) A TFT array substrate comprising:

a display area including a pixel electrode formed over a substrate;

a switching element connected to the pixel electrode;

a terminal electrode is formed outside of the display area for connecting to an external signal source;

a first conductive line extending from the terminal electrode to the display area;

a second conductive line connected to the terminal electrode and extending from the terminal electrode to the end of the substrate;

an insulating layer that is interposed between the first conductive line and the second conductive line, the insulating layer formed over the second conductive layer; and

wherein the second conductive line is connected to the terminal electrode via a contact hole formed in the insulating layer.

15. (Previously Presented) The TFT array substrate according to claim 14, wherein the first conductive line is formed over the insulating layer.

16. (Previously Presented) The TFT array substrate according to claim 14, wherein a passivation film is formed over the first conductive line and the first conductive line is connected to the terminal electrode via a contact hole formed in the passivation film.

17. (Previously Presented) The TFT array substrate according to claim 14, wherein the second conductive line is formed in a lower layer than the layer where the first conductive line is formed.

18. (Previously Presented) The TFT array substrate according to claim 14, wherein the first conductive line is connected to a gate electrode or a source electrode.

19. (Previously Presented) The TFT array substrate according to claim 14, wherein a passivation film is formed over the insulating layer so that the insulating layer is sandwiched between the passivation film and the second conductive layer.

20. (Previously Presented) The TFT array substrate according to claim 14, wherein the insulating layer is a gate insulating layer.

21. (Previously Presented) The TFT array substrate according to claim 14, wherein the second conductive line is directly connected to the terminal electrode.

22. (Previously Presented) The TFT array substrate according to claim 19, wherein the passivation film is further formed over the first conductive line.

23. (Currently Amended) The TFT array substrate according to claim 22, wherein the insulating layer includes a first part formed in the same layer as the layer where the fist conductive line is formed, a second part formed ~~over~~ beneath the first conductive line, and a part extending from the first part to the second part;

wherein the second conductive line is formed ~~over~~ beneath the first part of the first insulating layer; and

wherein the terminal electrode extending from over the first conductive line to over the second conductive line is connected to the first conductive layer via the contact hole formed in the passivation layer, and connected to the second conductive layer via a contact hole formed in the passivation layer and the insulating layer.

24. (Previously Presented) A TFT array substrate comprising;

a display area including a pixel electrode formed over a substrate;

a switching element connected to the pixel electrode;

a terminal electrode is formed outside of the display area for connecting to a signal source;

a first conductive line extending from the terminal electrode to the display area;

a second conductive line extending from the terminal electrode to the end of the substrate, the second conductive line formed in a lower layer than the layer where the first conductive line is formed; and

an insulating layer formed over the second conductive line,

wherein the second conductive line is not directly connected to the first conductive line.

25. (Previously Presented) The TFT array substrate according to claim 24, wherein a passivation layer is disposed over the insulating layer.

26. (Previously Presented) The TFT array substrate according to claim 24, wherein the insulating layer is a gate insulating layer.

27. (Previously Presented) The TFT array substrate according to claim 14, wherein the first conductive line and the terminal electrode are connected via a plurality of contact holes.

28. (Previously Presented) The TFT array substrate according to claim 27, wherein the plurality of contact holes are provided near the end of the side of the display area of the terminal electrode and near the end of the substrate of the first conductive line.

29. (Previously Presented) The TFT array substrate according to claim 14, wherein the width of the second conductive line becomes thin near the end of the side of the substrate end of the terminal electrode.

30. (Previously Presented) A display device comprising the TFT array substrate of claim 14.

31. (Previously Presented) A display device comprising the TFT array substrate of claim 24.